CLAIMS

What is claimed is.

1. A process of forming a memory device, comprising:

forming a first topology over a substrate;

forming a subsequent topology over the first topology;

forming a first memory structure at the first topology; and

forming at least one subsequent memory structure at a corresponding at least one subsequent topology.

2. The process according to claim 1, wherein the memory device includes a ferroelectric memory device.

3. The process according to claim 2, wherein forming at least one subsequent memory structure further includes:

forming a second topology;

forming a second memory structure at the second topology;

forming an interlayer dielectric (ILD) layer over the second memory structure;

forming a third topology above the ILD layer ; and

forming a third memory structure at the third topology.

4. The process according to claim 2, wherein forming at least one subsequent memory structure further includes:

forming a second topology;

forming a second memory structure at the second topology, wherein the second memory structure is formed comprising:

forming a ferroelectric layer over the first memory structure;

forming a conductive layer over the layer;

planarizing the conductive layer; and

patterning the conductive layer to form a third electrode; and

forming an interlayer dielectric (ILD) layer over the second memory structure;

forming a third topology above the ILD layer ; and

forming a third memory structure at the third topology.

5. The process according to claim 2, wherein forming a first memory structure further includes:

forming a first electrode over the substrate;

forming a first memory layer over the first electrode; and

forming a second electrode over the first memory layer.

6. The process according to claim 2, wherein forming a first memory structure and forming a subsequent memory structure further includes:

forming a first electrode over the substrate;

forming a first memory layer over the first electrode;

forming a second electrode over the first memory layer;

forming a second memory layer over the second electrode; and

forming a third electrode over the second memory layer.

7. A process of forming a ferroelectric polymer memory device, comprising:

forming a first topology above a substrate;

forming a subsequent topology over the first topology;

forming a first ferroelectric polymer memory structure at the first topology; and

forming at least one subsequent ferroelectric polymer memory structure at a corresponding at least one subsequent topology.

8. The process according to claim 7, wherein forming a subsequent ferroelectric polymer memory structure further comprises:

forming a second topology;

forming a second ferroelectric polymer memory structure at the second topology;

forming an interlayer dielectric (ILD) layer over the second ferroelectric polymer memory structure;

forming a third topology above the ILD layer ; and

forming a third ferroelectric polymer memory structure at the third topology.

9. The process according to claim 7, wherein forming a subsequent ferroelectric polymer memory structure further comprises:

forming a second topology;

forming a second ferroelectric polymer memory structure at the second topology, wherein the second ferroelectric polymer memory structure is formed comprising:

forming a ferroelectric polymer layer over the first ferroelectric polymer memory structure;

forming a conductive layer over the ferroelectric polymer layer;

planarizing the conductive layer; and

patterning the conductive layer to form a third electrode; and

forming an interlayer dielectric (ILD) layer over the second ferroelectric polymer memory structure;

forming a third topology above the ILD layer ; and

forming a third ferroelectric polymer memory structure at the third topology.

10. The process according to claim 7, wherein forming a first ferroelectric memory structure further comprises:

forming a first electrode over the substrate;

forming a first ferroelectric memory layer over the first electrode; and

forming a second electrode over the first ferroelectric memory layer.

11. The process of forming a memory device according to claim 7, wherein forming a first ferroelectric polymer memory structure and forming a subsequent ferroelectric polymer memory structure further comprises:

forming a first electrode over the substrate;

forming a first ferroelectric polymer memory layer over the first electrode;

forming a second electrode over the first ferroelectric polymer memory layer;

forming a second ferroelectric polymer memory layer over the second electrode; and

forming a third electrode over the second ferroelectric polymer memory layer.

12. The process of forming a polymer memory device according to claim 7, wherein forming a ferroelectric polymer memory structure comprises forming a layer selected from spin-on depositing, chemical vapor depositing, substrate dip depositing, Langmuir-Blodgett depositing, and spray-on depositing.

13. A process of forming a ferroelectric oxide memory device, comprising:

forming a first topology above a substrate;

forming a subsequent topology over the first topology;

forming a first ferroelectric oxide memory structure at the first topology; and

forming at least one subsequent ferroelectric oxide memory structure at a corresponding at least one subsequent topology.

14. The process according to claim 13, wherein forming a subsequent ferroelectric oxide memory structure further comprises:

forming a second topology;

forming a second ferroelectric oxide memory structure at the second topology;

forming an interlayer dielectric (ILD) layer over the second ferroelectric oxide memory structure;

forming a third topology above the ILD layer ; and

forming a third ferroelectric oxide memory structure at the third topology.

15. The process according to claim 13, wherein forming a subsequent ferroelectric oxide memory structure further comprises:

forming a second topology;

forming a second ferroelectric oxide memory structure at the second topology, wherein the second ferroelectric oxide memory structure is formed comprising:

forming a ferroelectric oxide layer over the first ferroelectric oxide memory structure;

forming a conductive layer over the ferroelectric oxide layer;

planarizing the conductive layer; and

patterning the conductive layer to form a third electrode; and

forming an interlayer dielectric (ILD) layer over the second ferroelectric oxide memory structure;

forming a third topology above the ILD layer ; and

forming a third ferroelectric oxide memory structure at the third topology.

16. The process according to claim 13, wherein forming a first ferroelectric oxide memory structure further comprises:

forming a first electrode over the substrate;

forming a first ferroelectric oxide memory layer over the first electrode; and

forming a second electrode over the first ferroelectric oxide memory layer.

17. The process of forming a memory device according to claim 13, wherein forming a first ferroelectric oxide memory structure and forming a subsequent ferroelectric oxide memory structure further comprises:

forming a first electrode over the substrate;

forming a first ferroelectric oxide memory layer over the first electrode;

forming a second electrode over the first ferroelectric oxide memory layer;

forming a second ferroelectric oxide memory layer over the second electrode; and

forming a third electrode over the second ferroelectric oxide memory layer.

18. The process according to claim 13, wherein forming a ferroelectric oxide memory structure comprises forming a layer selected from chemical vapor deposition, spin-on deposition, and physical vapor deposition.

19. A ferroelectric memory device comprising:

a first topology disposed over a substrate;

a first ferroelectric structure disposed in the first topology; and

a subsequent topology disposed over the first topology, and a subsequent ferroelectric structure disposed in the subsequent topology.

20. The ferroelectric memory device according to claim 19, wherein the first ferroelectric structure and a subsequent ferroelectric structure further comprise:

a first electrode disposed over the substrate;

a first ferroelectric polymer layer disposed over the first electrode;

a second electrode disposed over the first ferroelectric polymer layer;

a second ferroelectric polymer layer disposed over the second electrode; and

a third electrode disposed over the second ferroelectric polymer layer.

21. The ferroelectric memory device according to claim 20, wherein the electrodes have a width that is a minimum feature of a photolithography technology, selected from 0.25 micron, 0.18 micron, 0.13 micron, and 0.11 micron.

22. The ferroelectric memory device according to claim 20, wherein the first ferroelectric structure and a subsequent ferroelectric structure further comprise:

a first electrode disposed over the substrate;

a first ferroelectric oxide layer disposed over the first electrode;

a second electrode disposed over the first ferroelectric oxide layer;

a second ferroelectric oxide layer disposed over the second electrode; and

a third electrode disposed over the second ferroelectric oxide layer.

23. The ferroelectric memory device according to claim 21, wherein the electrodes have a width that is a minimum feature of a photolithography technology, selected from 0.25 micron, 0.18 micron, 0.13 micron, and 0.11 micron.

24. A system, comprising:

a processor;

a ferroelectric memory system coupled to the processor;

an input/output (I/O) circuit coupled to the processor and the ferroelectric memory system; and

the ferroelectric memory system including:

a substrate;

a first topology disposed over the substrate;

a first ferroelectric structure disposed in the first topology; and

a subsequent topology disposed over the first topology, and a subsequent ferroelectric structure disposed in the subsequent topology.

25. The system according to claim 24, wherein the processor is disposed in a host selected from a clock, a television, a cell phone, a personal computer, an automobile, an industrial control system, and an aircraft.

26. The system according to claim 24, wherein the ferroelectric memory structure is selected from a ferroelectric polymer memory structure and a ferroelectric oxide memory structure.

27. The system according to claim 24, wherein the processor comprises a CMOS logic region disposed in the substrate, and wherein the ferroelectric memory system comprises a die in a memory module.

28. The system according to claim 24, wherein the processor comprises logic in a memory controller, and wherein the ferroelectric memory system comprises a die in a memory module.

29. The system according to claim 24, wherein the ferroelectric memory system comprises a chip in a chipset.